(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 547 815 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent: 12.03.1997 Bulletin 1997/11

(51) Int Cl.6: H01L 21/60, H01L 21/288

(21) Application number: 92311095.1

(22) Date of filing: 04.12.1992

(54) **Pseudo-electroless, followed by electroless, metallization of nickel on metallic wires, as for semiconductor chip-to-chip interconnections**

Pseudo-stromlose Plattierung, gefolgt durch stromlose Plattierung für die Metallisierung von Nickel auf metallischen Drähten, verwendet für die Interkonnektion vom Typen "chip-to-chip"

Pseudo-dépôt chimique, suivi d'un dépôt chimique pour la métallisation de nickel sur des fils métalliques, utilisés pour l'interconnexion du type "chip-to-chip"

(84) Designated Contracting States: DE FR GB NL

(30) Priority: 17.12.1991 US 809694

(43) Date of publication of application: 23.06.1993 Bulletin 1993/25

(73) Proprietor: AT&T Corp.
New York, NY 10013-2412 (US)

(72) Inventors:
- Bentson, Richard Soren
  Somerville, New Jersey 08876 (US)
- Rubin, Jerry Jay
  Chatham, New Jersey 07928 (US)
- Stepniak, Frank
  Minneapolis, Minnesota 55416 (US)

(74) Representative: Johnston, Kenneth Graham et al
Lucent Technologies (UK) Ltd,
5 Mornington Road
Woodford Green Essex, IG8 OTU (GB)

(56) References cited:
WO-A-91/08586

- JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 139, no. 2, February 1992, Manchester, New Hampshire, US, pp. 633-638; V.M. DUBIN : 'Selective Electroless Ni-Cu(P) Deposition for Via Hole Filling and Conductor Pattern Cladding in VLSI Multilevel Interconnection Structures'
- IEEE ELECTRON DEVICE LETTERS, vol. 10, no. 6, June 1989, New York, US, pp. 257-259; Pei-Lin PAI et al.: 'Selectively Deposited Nickel Film for Via Filling'

Printed by Jouve, 75001 PARIS (FR)

Description

This invention relates to methods of plating nickel on a limited portion of a patterned metallic layer, and finds application in the formation of semiconductor chip-to-chip inter-connections—also known as high, density interconnects for advanced VLSI (very large scale integration) packaging.

Semiconductor VLSI chips can contain in excess of a million transistors, together with hundreds of I/O (input/output) pads. To each of the pads, one or more chip-to-chip metallic interconnections ("interconnects") are attached, whereby a VLSI package is formed. The package typically contains as many as eight or more of these thus interconnected semiconductor VLSI chips.

The above-mentioned (metallic) interconnects are typically copper stripes ("lines" or "wires"), each of which runs along one of two or more metallization levels (horizontal planes), each level being separated from the next by a suitable insulating layer, such as a layer of polyimide. Wires that are located on two successive metallization levels are connected to one another through holes (apertures; "vias") in the insulating layer filled with a suitable metal. Each via thus has a height that is equal to the thickness of the insulating layer, typically in the approximate range between 5 and 10 μm, and the cross section of a via is typically 10 to 200 μm in diameter. Each of the wires on the top level typically is connected to one or more I/O pads of one or more chips, typically by means of a glob ("bump") of solder.

The paper entitled, "High Density Interconnect for Advanced VLSI Packaging" by A. C. Adams et al. published in Diffusion Processes in High Technology Materials, Proceedings of the ASM Symposium, pp. 129-136 (October 1987), describes a VLSI package in which the wires are made of copper, because of its desirably high electrical conductivity, and the insulating layer is polyimide because of its excellent dielectric and mechanical properties. Because the polyimide does not adhere well to copper, however, if a copper wire comes in direct physical contact with the polyimide, then undesirable delamination of the polyimide from the copper wire would occur, whereby the structure would be mechanically unreliable. Moreover, because of potential chemical interaction of copper with polyimide, if copper in either the wires or the vias would be in direct physical contact with the polyimide, then the insulating properties of the polyimide would be deteriorated. On the other hand, because nickel has good adherence properties with respect to, and is desirably non-interactive with, polyimide; therefore, the aforementioned paper teaches that the copper wires are to be coated with nickel, and the vias are to be filled also with nickel (to form nickel "plugs").

More specifically, to obtain such a structure, the nickel could be deposited into the apertures by two electroless steps--i.e., successive immersions in aqueous solutions ("plating baths") containing nickel ions, one such immersion before the polyimide layer has been formed, and the other such immersion after the polyimide layer has been formed and has been supplied with the apertures. The first immersion would coat the copper wires with nickel; the second immersion would thus produce the nickel plugs. However, we have found that the required compositions of the plating baths for the two immersions must be different. More specifically, a plating bath that is suitable for electroless plating the copper wires with nickel is not suitable for filling the vias with nickel (plugs), especially in view of the required height of each nickel plug to fill each via. Thus, the resulting electroless deposited nickel formed during the first immersion is necessarily dissimilar in composition to the nickel deposited during the second immersion, whereby the (second) nickel in the vias deposits poorly (if at all) on first nickel layer that coats the (top and side) surfaces of the copper; consequently, the subsequently formed nickel plugs undesirably do not reliably fill the vias. At the same time undesirably poor adhesion of copper to the polyimide tends to result, whereby moisture can undesirably migrate from the environment to the various levels and undesirably cause corrosion of the metallization.

Another approach is forming a thin nickel layer on copper by means of a quick ("flash") electroless process in a first plating bath, and using the resulting thin nickel layer as a foundation for a second, thick nickel layer deposited on this thin nickel layer by means of a second electroless process in a second plating bath having a composition that is different from that of the first bath, followed by forming the polyimide layer with its apertures filled with nickel plugs formed by means of an electroless process in a third plating bath having the same composition as that of the second bath. We have found that such a ("flash") electroless nickel layer also tends not to be a reliable foundation for the thick nickel layer and hence for the subsequent formation of the nickel plugs, again because of the required different composition of the two plating baths--one for the thin ("flash") nickel layer, and the other for the (overlying) thick nickel layer. That is, the thick nickel layer, as deposited on the thin ("flash") nickel layer, tends to be non-uniform in thickness, whereby at least some of the vias undesirably are not filled with metal and hence at least some of the desired electrical connections between successive metallization levels are undesirably non-existent.

Moreover, we have found that the use of electroplating (battery-assisted plating) as a process for coating the copper wires with nickel tends to produce an electroplated layer (of nickel on copper) that has an undesirably nonuniform thickness. Also, electroplating cannot be used at all to form the nickel plugs because at the time these plugs are to be formed it is simply not feasible to electrically access all the copper wires.

Therefore, it would be desirable to have a method of plating nickel on copper (wires)--the nickel having properties that enable reliable electroless formation of

nickel, for example, in an aperture in an overlying insulating layer.

In a paper entitled "Selectively Deposited Nickel Film for Via Filling" published in IEEE Electron Device Letters, vol. 10, no. 6, pp.257-259 (June 1989), and in International Application Published Under the Patent Cooperation Treaty WO 91/08586 (published 13 June 1991) entitled "Method of Plating Into Holes and Products Thereby"--techniques and devices are described for using palladium, plated on aluminum wiring, as a catalyst for the subsequent electroless plating of nickel in a via (hole), the via being located in an insulating layer overlying the aluminum wiring.

According to this invention there is provided a method as claimed in claim 1.

As used herein, the term "electrical contact" includes, but is not limited to, intimate (direct) physical contact of the surface of one metallic layer with the other.

In the above sequence of steps, step (a) of claim 1 is called a "pseudo-electroless" nickel plating process, since this step (a) does not involve any externally applied voltages or currents (as does electroplating) but it does require electrical contact with the auxiliary metal layer, which advantageously comprises nickel (in contradistinction to purely electroless plating, which does not require any contact with any auxiliary metal layer).

Step (b) of claim 1 is required to prevent short circuits among the various wires formed by the first patterned metallic layer.

Brief Description of the Drawing

FIGS. 1-4 depict elevational side views in cross section of various stages in the fabrication of semiconductor chip-to-chip interconnections including the step of pseudo-electroless metallization followed by electroless metallization.

Only for the sake of clarity, none of the Figures is drawn to any scale.

Detailed Description

In FIG. 1, structure 100 represents an early stage in the fabrication of semiconductor chip-to-chip interconnections. The structure 100 is formed by a silicon wafer 10 that is heavily doped, typically with boron, in order to provide high electrical conductivity. The bulk resistivity of the silicon wafer 10 typically is less than 0.001 ohm-cm.

Upon the bottom surface of the silicon wafer 10 is located a silicon dioxide layer 9 and a silicon nitride layer 8. The thickness of the silicon dioxide layer 9 typically is approximately equal to 0.05 μm, and the thickness of the silicon nitride layer 8 is approximately equal to 0.120 μm. The silicon dioxide layer 9 is formed simultaneously with the thin (0.05 μm) portions of the silicon dioxide layer 11, and the silicon nitride layer 8 is formed simultaneously with the silicon nitride layer 12. Ultimately, in the final structure, the silicon dioxide layer 9 and the silicon nitride layer 8 will be removed and be replaced by a metallic layer, such as copper, for providing a good ground contact for the silicon wafer 10.

Upon the top major surface of the silicon wafer 10 are located a silicon dioxide layer 11, a 0. 120 μm thick silicon nitride layer 12 deposited by low pressure chemical vapor deposition, a 0.055 μm thick deposited titanium layer 13, a 0.065 μm thick deposited chromium layer 14, a 0.250 μm thick sputter-deposited copper layer 15, a 0.055 μm thick deposited and patterned titanium layer 16, a 2.5 μm thick patterned photoresist layer 17 having an aperture that was used for patterning by liquid etching on originally unpatterned titanium layer (not shown) to form the patterned titanium layer 16, and a patterned copper layer 18 filling the aperture in the patterned photoresist layer 17. Typically, the aperture in the patterned photoresist layer 17 was formed by means of exposing an initially uniformly thick spun-on resist layer to a patterning ultraviolet beam, followed by standard wet development of the photoresist layer.

The thickness of the silicon dioxide layer 11 is typically approximately equal to 1.0 μm except at areas underlying central portions of the patterned copper layer 18 where the thickness of the silicon dioxide layer 11 is approximately equal to 0.05 μm. The purpose of the thin oxide is to provide a desirably high capacitance between the copper layer 18, which will serve as a power plane, and the silicon wafer 10, which will be grounded.

In case the patterned copper layer 28 (FIGS. 3 and 4) to be formed from the patterned copper layer 18 is to serve as a signal line, then the underlying silicon dioxide layer is advantageously everywhere equal to approximately 1.0 μm. And in case it is to serve as part of a vertical ground connection running from the silicon wafer 10 to an overlying silicon integrated circuit chip, then the thickness of both the silicon dioxide layer 11 and the silicon nitride layer are zero, in order to enable proper electrical contact to ground. Advantageously the patterned copper layer 18 is formed by electroplating (of copper onto the copper layer 15) within the aperture of the patterned photoresist layer 17, after removing (not shown in FIG. 1) an edge region of the photoresist layer 17 to expose an edge region of the patterned titanium layer 16, to supply an electrode for the electroplating process.

The sputter-deposited copper layer 15 is useful because electroplated copper would not adhere very well to the chromium layer 14, whereas (in vacuo) sputter-deposited copper does. On the other hand, the chromium layer 14 is useful for the pseudo-electroless deposition of the nickel layer 29 (FIG. 3) which, in turn, because of its high quality (uniform thickness) is useful as a good foundation for a subsequent electroless deposition of the nickel layer 31 (FIG. 4). The titanium layer 13 is useful because the chromium layer 14 does not adhere well to the underlying silicon nitride layer 12; the titanium layer 16 is useful because the photoresist layer

17 does not adhere well to the underlying copper layer 15. The patterning of the photoresist layer 17 is made to be such that the copper layer 18 is patterned in accordance with the desired routing of the resulting copper wire formed by the patterned copper layer 28 (FIG. 3).

After the patterned copper layer 18 has been formed, the photoresist layer 17 is removed. Then the remainder of the titanium layer 16 is removed, as by liquid etching in aqueous HF. Next, the (relatively thin) copper layer 15 is removed, as by liquid etching in aqueous H_2SO_4 and H_2O_2, whereby the thickness of the patterned (relatively thick) copper layer 18 is reduced, but only by a relatively small amount in comparison to its original thickness. In this way, a patterned copper layer 28,25 is formed (FIG. 2). This copper layer 28,25 will serve as a power-carrying line ("power plane") that transports a voltage supply (V_{DD}) to an overlying silicon chip (not shown). Thus the power plane must be insulated from a ground connection (not shown) running vertically from the top surface of the silicon wafer 10 at a location (not shown) where the insulating layers 11 and 12 have been removed. Therefore, the patterned copper layer 28,25 must be patterned, i.e., cannot overlie the entire top surface of the wafer 10. Thus, the stage of fabrication represented by the structure 100 (FIG. 1) is attained.

This structure 100 is then immersed in a nickel plating bath 45, that is, an aqueous solution containing nickel ions and advantageously also hypophosphite ions. Other advantageous ingredients in the bath 45 include stabilizers, buffers, accelerators, complexors, and wetting agents. Components, together with instructions for making such a plating bath, are sold under the name "Nicklad-1000" by WITCO Company. The plating bath 45 is contained in a container 44. More specifically, the structure 100 while located in the bath 45, is mechanically squeezed between an auxiliary metallic layer 41, typically steel coated with nickel, and an insulating teflon layer 40. Typically, this auxiliary metal layer pair 41 is part of a cassette that holds one or more such structures 100 firmly in place.

During the immersion, nickel tends to plate onto the external metal layer 41 as well as onto exposed surfaces of the copper layer 28,25. Advantageously, opposing forces 42 and 43, applied to the auxiliary metallic layer 41 and the insulating layer 40, respectively, maintain the top surface of the extended chromium layer 14 in intimate (direct) physical contact with the bottom surface of the (nickel-coated) auxiliary metallic layer 41. In this way, a patterned pseudo-electroless nickel layer 29.1 begins to form on the exposed top and side surfaces of the copper layer 28,25, whereby the stage of fabrication represented by the structure 100 (FIG. 2) is attained. At the same time, no nickel will deposit on the chromium layer 14 because of lack of affinity, as well as because of a protective oxide passivation layer that tends to form on the surface of the chromium layer 14. After a sufficient amount of time has elapsed, a desired thickness of typically about 0.50 μm of pseudo-electroless nickel is thus deposited, whereby the desired patterned pseudo-electroless nickel layer 29 (FIG. 3) is thus formed. This pseudo-electroless layer 29 forms a desirably uniformly thick coating of nickel on the top and side surfaces of the patterned copper layer 28.

Alternatively, the function of the auxiliary metallic layer 41 (as an electrode) can be served by a nickel layer that has been formed (prior to the immersion of the structure 100 in the bath 45) by means of depositing nickel on an exposed portion of the surface of the chromium layer 14, i.e., on a portion of the chromium layer external to the patterned copper layer 28,25.

Next, the entire thickness of the chromium layer 14 is removed (as by immersion in an aqueous solution of $KMnO_4$ and NaOH) except for portions protected by the overlying patterned copper layer 28. Then the titanium layer 13 is wet etched, as by an aqueous solution of HF, also except for portions underlying the copper layer 28. In this way, underlying the patterned copper layer 28, a patterned chromium layer 24 overlying a patterned titanium layer 23 (FIG. 3) is formed, and the stage of fabrication represented by the structure 300 is attained.

Next, the top surface of the structure 300 is coated with a polyimide layer 30 (FIG. 4) that has a thickness of typically about 10 μm and has an aperture overlying a limited portion of the top surface of the pseudo-electroless nickel layer 29. This limited portion extends into the plane of the drawing (FIG. 4) only so far as is desired for a via between the first and second level metallizations. Viewed from the top, the via is typically the area of a circle having a diameter in the approximate range of between 30 and 100 μm. The structure is then immersed in a (electroless) nickel plating bath--which advantageously can be the same as the bath 45 that was previously used for forming the pseudo-electroless nickel layer 29--whereby an electroless nickel plug 31 is formed to fill the aperture in the polyimide layer.

Next, a patterned chromium layer 34, 54 (FIG. 4), patterned copper layers 38, 35, and 58, 55, and patterned pseudo-electroless nickel layers 39, 59 are formed in the same manner as the patterned chromium layer 24, the patterned copper layer 28, 25, and the patterned pseudo-electroless layer 29 were formed. No titanium layer is formed (as the counterpart of the titanium layer 13) between the top surface of the polyimide layer 30 and the patterned chromium layer 34, 54, because titanium is not needed for good adherence of the patterned chromium layer 34, 54 to the polyimide layer 30; on the contrary, titanium would cause its own adherence problems with respect to the polyimide layer 30. On the other hand, a patterned titanium layer--the counterpart of the patterned titanium layer 16--is indeed formed on the top surface of the patterned copper layer 35, 55 before patterning, for the same reasons as the patterned titanium layer 16 was needed. Then, after forming another polyimide layer 50 with apertures overlying the patterned copper layer 38, 58, electroless nickel plugs

51 and 61 are formed in these apertures in the same manner as the electroless nickel plug 31 was formed.

Thus the stage of fabrication represented by the structure 400 is attained in which the electroless nickel plug 51 serves as a vertical connection for power from the second level of metallization--viz., the patterned copper layer 38--to the third level of metallization (not shown). Thus, the vertically-running electrical connection formed by the nickel plug 31, the chromium layer 34, the copper layers 38 and 35, the (pseudo-electroless) nickel layer 39 and the (electroless) nickel plug 51 together form a part of a desired electrical connection from the power line 28 to an overlying VLSI chip (not shown). The electroless nickel plug 61 serves as a vertical connection for signal from the second level of metallization--viz., the patterned copper layer 58.

The patterned copper layers 28, 38, and 58 will run horizontally, i.e., on a fixed metallization level, in paths consistent with the routing desired for that level. In this way, in the scheme exemplified by the structure 400 these patterned copper layers serve as the desired copper power planes (e.g., 28), copper plugs (e.g., 38) or copper signal wires (e.g., 58) on the various metallization levels, as the case may be.

Although the invention has been described in detail with respect to a specific embodiment the following modifications can be made without departing from the scope of the invention. Instead of copper wires, aluminum, gold, or silver wires can be used ; and the pseudo-electroless, followed by electroless, nickel can be plated on them for connecting wires located on one level of metallization to wires located on another level. Instead of chromium, other metals such as tungsten, molybdenum, tantalum, or other refractory metals that form dense passivating (protective oxide) layers can be used for the extended metallic layer 14--and thus for the layers 24, 34, and 54. Also, instead of nickel, the external metallic layer 41 can be coated with such other metals such as gold, platinum, palladium, or zinc.

Moreover, in an embodiment not forming part of the claimed invention during an initial phase of the formation of the nickel layer 29 (as well as the nickel layers 39 and 59--i.e., any of the pseudo-electroless layers), the deposition of nickel can be battery-assisted (electroplated) in the aforementioned bath used for the pseudo-electroless nickel deposition. After this battery-assisted process has resulted in the formation of a nickel layer that everywhere coats the copper wires (to a thickness of nickel advantageously in the approximate range of between 0.07 and 0.10 μm, for the sake of uniformity of thickness), the battery is removed (the external electric circuit is broken) and the pseudo-electroless nickel plating process is implemented to complete the thickness (typically approximately 0.5 μm) of the nickel layer 29: a purely electroplated nickel layer having the thickness desired for the nickel layer 29 tends to have an undesirably non-uniform thickness.

Thus, the nickel plating process for forming the nickel layer 29 can have an initial electroplating phase whose time duration (as can be determined by experiment) is a specified fraction of the entire deposition time of the nickel layer 29. During the battery-assisted phase, the positive pole of the battery (or other d-c source) is connected to a wire or electrode that is dipped in the plating bath, while the negative pole of the battery is connected directly to the extended chromium layer 14 or to the auxiliary metallic layer 41 (and hence, indirectly, is electrically coupled to the chromium layer 14). Conveniently, the subsequent pseudo-electroless process (i.e., the process which is implemented after completion of the nickel deposition by means of the initial electroplating) can be implemented by disconnecting the battery (or other d-c source) and connecting (shorting) together the two wires (that were needed for connections to the battery) emerging from the plating bath. Thus the term "pseudo-electroless plating" includes the situation (FIG. 2) in which the extended chromium layer 14 is not in direct physical contact with an external nickel layer but is in electrical contact with it through a wire that the chromium layer 14 touches. The foregoing technique, involving an initial phase of electroplating followed by a final phase of pseudo-electroless plating to form the nickel layer 29, is useful in cases where the semiconductor wafer 10 is not in any direct physical contact with a conductive portion (if any) of the cassette or other holding means that keeps the wafer in place in the plating bath. Advantageously, the portion of the thickness of the nickel layer 29 thus formed during the final phase is at least one-half that formed during the initial phase (of electroplating).

Claims

1. A method of plating nickel on a limited portion of a first patterned metallic layer (25, 28) located overlying a limited portion of a first insulating layer (11, 12), the first patterned metallic layer being separated from the first insulating layer initially by an extended metallic layer (14), comprising the steps of:

    (a) forming a second metallic layer (29) comprising nickel on the first patterned metallic layer by immersing the first patterned metallic layer in an aqueous solution (45) comprising nickel ions,
    (b) removing the extended metallic layer except in regions underlying the first patterned metallic layer;
    (c) forming a second insulating layer (30), overlying the first patterned metallic layer and the first insulating layer, and forming an aperture therein overlying the limited portion of the first patterned metallic layer; and
    (d) forming a third metallic layer (31) comprising nickel on the second metallic layer by an

electroless plating process, whereby the aperture in the second insulating layer is filled with nickel;

CHARACTERIZED IN THAT

the order of sequence of steps is (a), (b), (c), and (d), and **IN THAT**
during step (a) the first patterned metallic layer intimately physically contacts the extended metallic layer (14), and the extended metal layer electrically contacts an auxiliary metallic layer (41) at least a portion of which is immersed in the aqueous solution.

2. A method as claimed in claim 1 wherein
the first patterned metallic layer (28, 25) is formed by an initial step of sputter-depositing a copper layer (18) on the top surface of the extended metallic layer (14) prior to step (a), and the copper layer 18 is patterned prior to (a).

3. A method as claimed in claim 2 comprising the steps of:

forming a third patterned metallic layer (16) on the top surface of the copper layer (15);
forming a patterned auxiliary insulating layer (17) on the top surface of the third patterned metallic layer having at least one aperture, whereby a patterned sixth metallic layer (16) is formed and whereby the portion of the copper layer (15) located underlying the aperture in the patterned auxiliary insulating layer (17) is exposed;
electroplating a metal layer comprising copper into the aperture of the patterned auxiliary insulating layer (17), whereby a copper layer (18) is formed contacting the portion of the copper layer (15) located at the bottom of the aperture in the patterned auxiliary insulating layer (17);
removing the patterned auxiliary insulating layer (17);
removing the third patterned metallic layer (16); and
removing the complementary portion of the copper layer (15), which was not located underlying the aperture in the patterned auxiliary insulating layer (17), whereby the thickness of the copper layer (18) is reduced and whereby the first metallic layer (18, 25) is formed.

Patentansprüche

1. Verfahren zum Beschichten mit Nickel an einem begrenzten Abschnitt einer ersten strukturierten metallischen Schicht (25, 28), die über einem begrenzten Abschnitt einer ersten isolierenden Schicht (11, 12) liegt, wobei die erste strukturierte metallische Schicht von der ersten isolierenden Schicht anfänglich durch eine ausgedehnte metallische Schicht (14) getrennt ist, umfassend die Schritte des:

(a) Ausbildens einer zweiten metallischen Schicht (29) mit Nickel an der ersten strukturierten metallischen Schicht durch Eintauchen der ersten strukturierten metallischen Schicht in eine wässrige Lösung (45) mit Nickelionen,
(b) Entfernen der ausgedehnten metallischen Schicht mit Ausnahme der Bereiche, die unter der ersten strukturierten metallischen Schicht liegen,
(c) Ausbilden einer zweiten isolierenden Schicht (30), die über der ersten strukturierten metallischen Schicht und der ersten isolierenden Schicht liegt, und Ausbilden einer Öffnung darin, die über dem begrenzten Abschnitt der ersten strukturierten metallischen Schicht liegt und
(d) Ausbilden einer dritten metallischen Schicht (31) mit Nickel an der zweiten metallischen Schicht durch ein außenstromloses Beschichtungsverfahren, wobei die Öffnung in der zweiten isolierenden Schicht mit Nickel gefüllt wird,

dadurch gekennzeichnet, daß
die Reihenfolge der Schritte (a), (b), (c) und (d) ist, und daß während des Schrittes (a) die erste strukturierte metallische Schicht physikalisch eng die ausgedehnte metallische Schicht (14) kontaktiert und die ausgedehnte metallische Schicht eine metallische Hilfsschicht (41), von welcher wenigstens ein Teil in die wässrige Lösung eingetaucht ist, elektrisch kontaktiert.

2. Verfahren nach Anspruch 1, bei welchem die erste metallische Schicht (28, 25) durch einen anfänglichen Schritt des Sputterabscheidens einer Kupferschicht (18) an der oberen Oberfläche der ausgedehnten metallischen Schicht (14) vor dem Schritt (a) ausgebildet wird und die Kupferschicht (18) vor (a) strukturiert wird.

3. Verfahren nach Anspruch 2, umfassend die Schritte

des Ausbildens einer dritten strukturierten metallischen Schicht (16) an der oberen Oberfläche der Kupferschicht (15),
des Ausbildens einer strukurierten isolierenden Hilfsschicht (17) an der oberen Oberfläche der dritten strukturierten metallischen Schicht mit wenigstens einer Öffnung, wobei eine strukturierte sechste metallische Schicht (16) gebildet wird und wobei der Abschnitt der Kupferschicht (15), der unter der Öffnung in der strukturierten

isolierenden Hilfsschicht (17) liegt, freigelegt wird,
des außenstromlosen Beschichtens mit einer Metallschicht mit Kupfer in der Öffnung der strukturierten isolierenden Hilfsschicht (17), wobei eine Kupferschicht (18) ausgebildet wird, welche den Abschnitt der Kupferschicht (15), der an dem Boden der Öffnung in der strukturierten isolierenden Hilfsschicht (17) liegt, kontaktiert,
Entfemen der strukturierten isolierenden Hilfsschicht (17),
Entfemen der dritten strukturierten metallischen Schicht (16) und
Entfemen des komplementären Abschnitts der Kupferschicht (15), der nicht unter der Öffnung der isolierenden strukturierten Hilfsschicht (17) angeordnet war, wobei die Dicke der Kupferschicht (18) vermindert wird und wobei die erste metallische Schicht (18, 25) ausgebildet wird.

Revendications

1. Procédé de placage de nickel sur une partie limitée d'une première couche métallique (25,28) à motifs sus-jacente à une partie limitée d'une première couche isolante (11,12), la première couche métallique à motifs étant séparée de la première couche isolante initialement par une couche métallique étendue (14), comprenant les stades consistant :

   (a) à former une deuxième couche métallique (29) comprenant du nickel sur la première couche métallique à motifs en immergeant la première couche métallique à motifs dans une solution aqueuse (45) comprenant des ions nickel;
   (b) à éliminer la couche métallique étendue sauf dans des régions sous-jacentes à la première couche métallique à motifs;
   (c) à former une deuxième couche isolante (30), sus-jacente à la première couche métallique à motifs et à la première couche isolante, et à y former une ouverture, recouvrant la partie limitée de la première couche métallique à motifs; et
   (d) à former une troisième couche métallique (31) comprenant du nickel sur la deuxième couche métallique par un procédé de placage d'un dépôt chimique, de sorte que l'ouverture dans la deuxième couche isolante est remplie de nickel;

   caractérisé en ce que

   - l'ordre de la séquence des stades est (a), (b), (c) et (d), et en ce que
   - pendant le stade (a) la première couche métallique à motifs est en contact physique intime avec la couche métallique étendue (14), et la couche métallique étendue est en contact électrique avec une couche métallique auxiliaire (41) dont au moins une partie et immergée dans la solution aqueuse.

2. Procédé suivant la revendication 1, dans lequel :

   - la première couche métallique (28,25) à motifs est formée par un stade initial consistant à former un dépôt d'une couche (18) de cuivre par pulvérisation cathodique sur la face supérieure de la couche métallique étendue (14) préalablement au stade (a), et
   - la couche (18) de cuivre est impressionnée préalablement à (a).

3. Procédé suivant la revendication 2, comprenant les stades consistant à :

   - former une troisième couche métallique à motifs (16) sur la face supérieure de la couche (15) de cuivre;
   - former une couche isolante auxiliaire (17) à motifs sur la face supérieure de la troisième couche métallique à motifs ayant au moins une ouverture, de sorte qu'une sixième couche métallique (16) à motifs est formée et de sorte que la partie de la couche (15) de cuivre sous-jacente à l'ouverture dans la couche isolante auxiliaire (17) à motifs est mise à nu;
   - effectuer une électrodéposition d'une couche métallique comprenant du cuivre dans l'ouverture de la couche isolante auxiliaire (17) à motifs, de sorte qu'une couche (18) de cuivre est formée en contact avec la partie de la couche (15) de cuivre située au fond de l'ouverture dans la couche isolante auxiliaire (17) à motifs;
   - éliminer la couche isolante auxiliaire (17) à motifs;
   - éliminer la troisième couche métallique (16) à motifs; et
   - éliminer la partie complémentaire de la couche (15) de cuivre, qui n'était pas sous-jacente à l'ouverture dans la couche isolante auxiliaire (17) à motifs, de sorte que l'épaisseur de la couche (18) de cuivre est réduite et de sorte que la première couche métallique (18,25) est formée.

FIG. 1

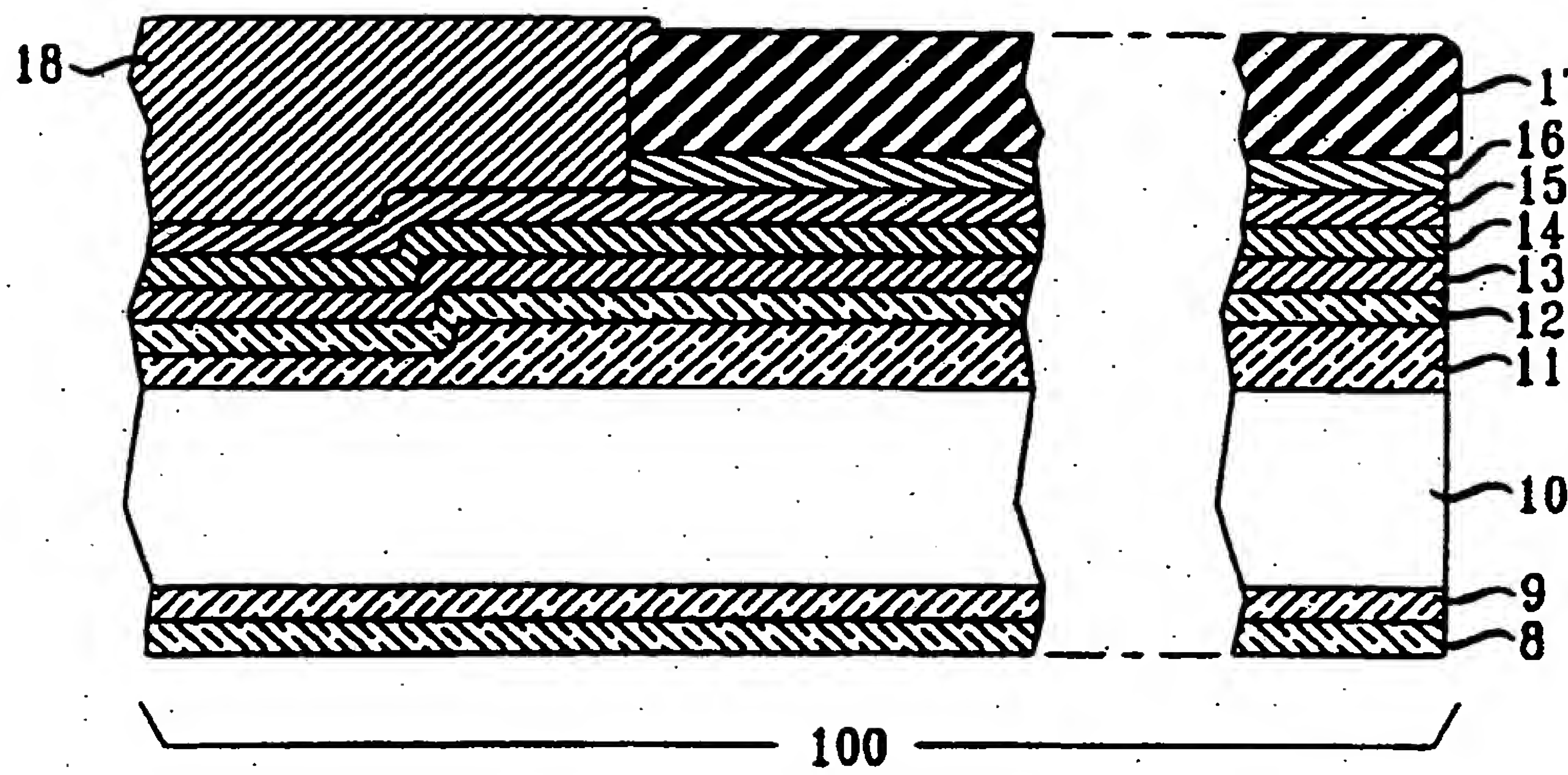

18
17
16
15
14
13
12
11
10
9
8
100

FIG. 2

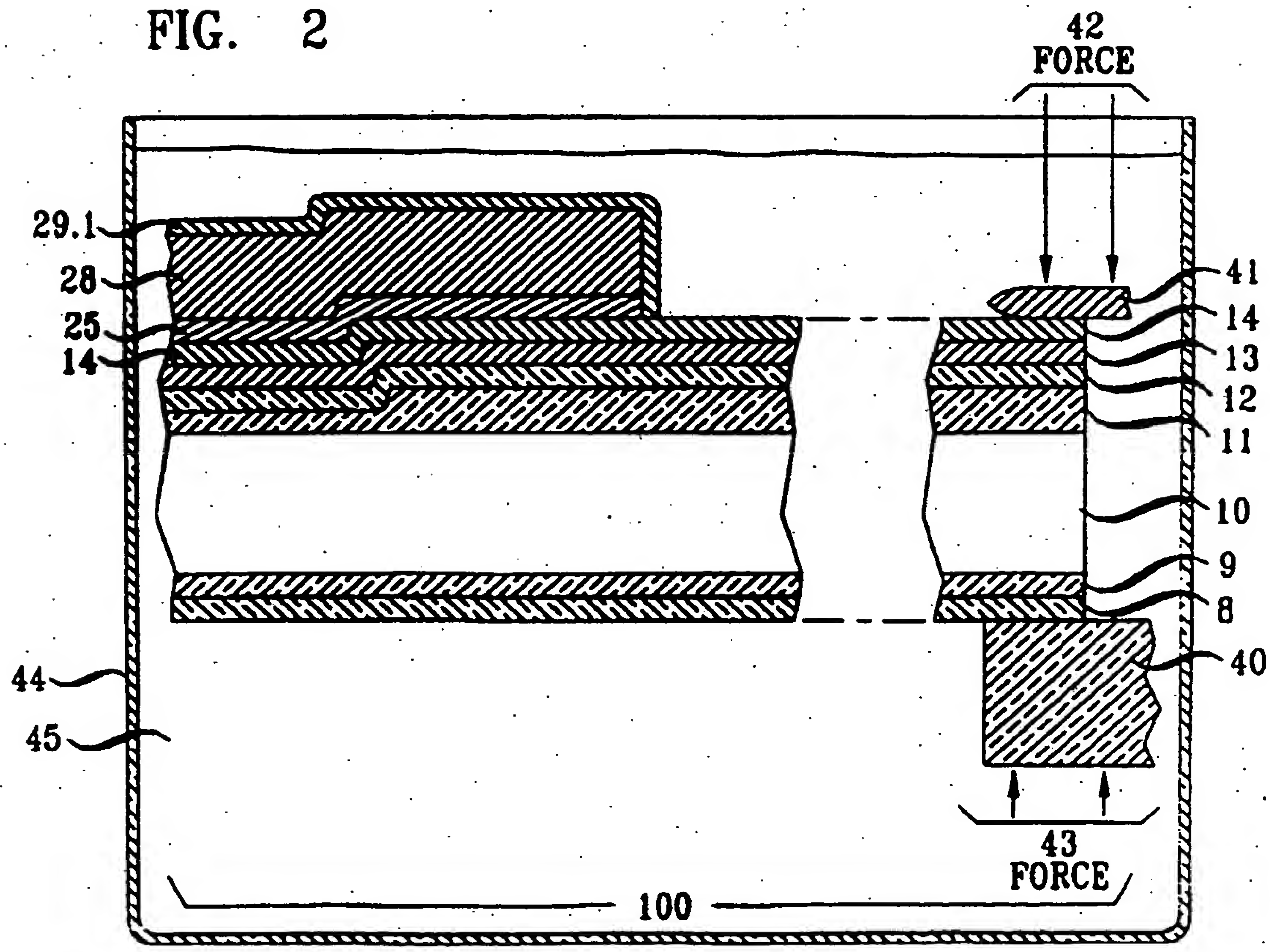

42
FORCE
29.1
28
25
14
41
14
13
12
11
10
9
8
40
44
45
43
FORCE
100

FIG. 3

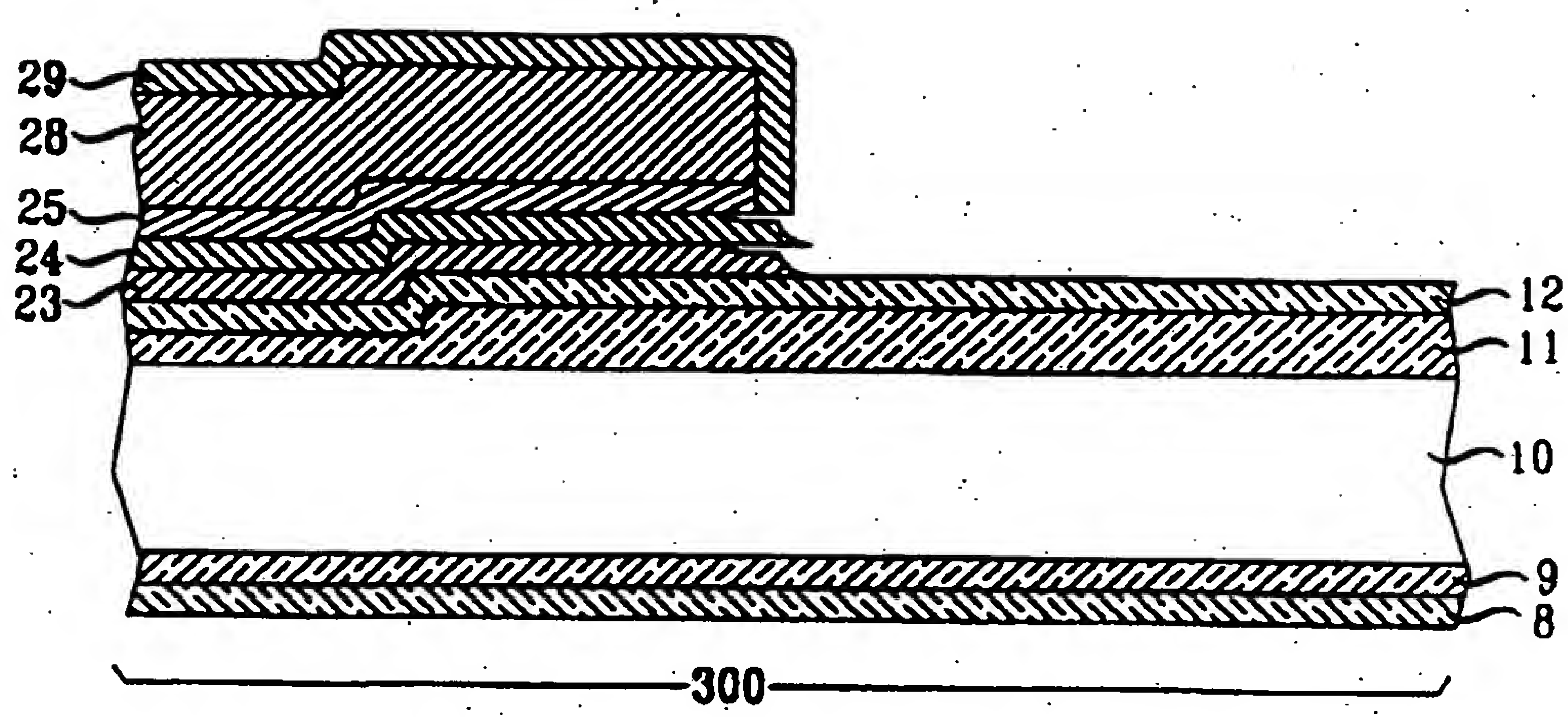
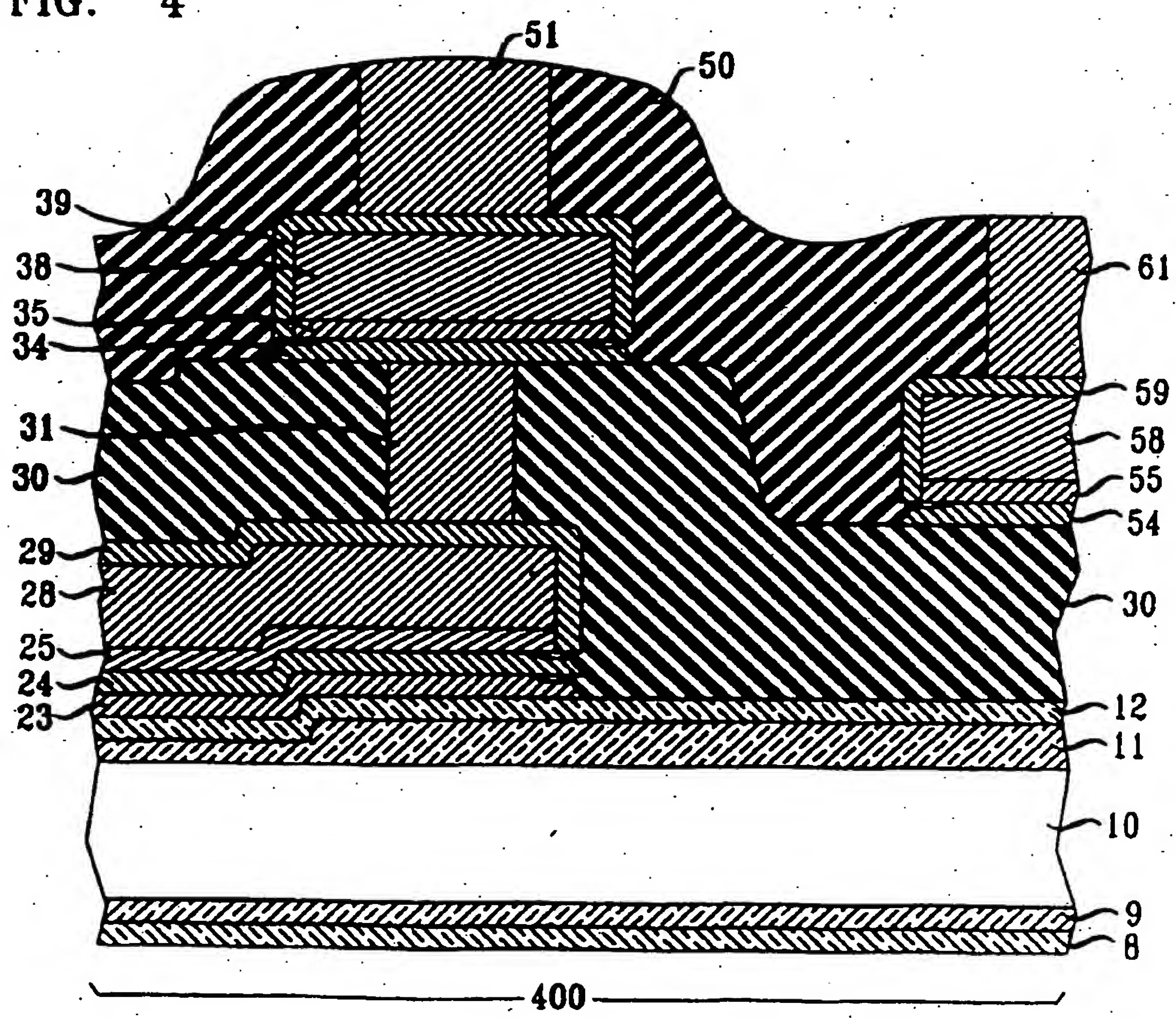

29
28
25
24
23
12
11
10
9
8
300

FIG. 4


51
50
39
38
35
34
31
30
29
28
25
24
23
61
59
58
55
54
30
12
11
10
9
8
400